IN THE ABSTRACT:

Please amend the Abstract of the Invention as follows:

A method for forming an electrical insulating layer on bit lines of the flash memory is disclosed. A conductive layer, a mask layer and a cap layer are sequentially formed on a semiconductor substrate and then are etched to form a plurality of ~~spacing~~ spacings. Afterwards, a dielectric layer is formed on the semiconductor substrate and a planarized layer is then formed on the dielectric layer. The planarized layer and the dielectric layer are etched sequentially wherein the etching rate of the planarized layer is less than that of the dielectric layer. Next, the dielectric layer is etched to remove a portion of the dielectric layer wherein the etching rate of the dielectric layer is higher than that of the cap layer, and thus a spacing dielectric layer is formed on the spacing. Thereafter, the cap layer is stripped wherein the etching rate of the dielectric layer is less than that of the mask layer so that the spacing dielectric layer has a round top and ~~slant~~ slanted sides. Finally, the mask layer is stripped and then the spacing dielectric layer remains to form the electrical insulating layer on bit lines of the flash memory.